CLAIMS

What is claimed is:

1. An apparatus for interrogating a data frame, the data frame comprising a plurality of bits, the apparatus comprising:

first logic, the first logic being configured to select a particular bit pattern in the data frame for interrogation;

second logic, the second logic being configured to compare a selected bit comparison value to said bit pattern to produce a comparison result; and

third logic, the third logic being configured to determine a location to which the comparison result is to be routed, and wherein one of said first, second and third logic is reconfigurable.

2. The apparatus of claim 1, wherein said first logic is reconfigurable to enable said first logic to alter the particular bit pattern selected from the data frame for interrogation.

3. The apparatus of claim 2, wherein the first logic is reconfigurable in real time.

4. The apparatus of claim 1, wherein the second logic is reconfigurable to enable said bit comparison value to be altered.

5. The apparatus of claim 4, wherein the second logic is reconfigurable in real time.

6. The apparatus of claim 1, wherein said third logic is reconfigurable to enable the location to which the comparison result is routed to be altered.

7. The apparatus of claim 6, wherein the third logic is reconfigurable in real time.

8. The apparatus of claim 4, further comprising:

fourth logic, the fourth logic being configured to resolve said comparison result into a single digital value and to output the single digital value to the third logic for routing by the third logic.

9. The apparatus of claim 8, further comprising:

fifth logic, the fifth logic being configured to select a particular bit pattern in the data frame for interrogation;

sixth logic, the sixth logic being configured to compare a selected bit comparison value to said particular bit pattern selected by the fifth logic to produce a comparison result; and

seventh logic, the seventh logic being configured to determine a location to which the comparison result produced by the sixth logic is to be routed, wherein one of said fifth, sixth and seventh logic is reconfigurable.

10. The apparatus of claim 9, wherein said fifth logic is reconfigurable to enable said fifth logic to alter the particular bit pattern selected from the data frame by the fifth logic for interrogation.

11. The apparatus of claim 9, wherein the sixth logic is reconfigurable to enable said bit comparison value to be altered.

12. The apparatus of claim 9, wherein said seventh logic is reconfigurable to enable the location to which the comparison result is routed to be altered.

13. The apparatus of claim 9, wherein said fifth logic is reconfigurable in real time to enable said fifth logic to alter, in real time, the particular bit pattern selected from the data frame by the fifth logic for interrogation.

14. The apparatus of claim 9, wherein said sixth logic is reconfigurable in real time in real time to enable said bit comparison value to be altered in real time.

15. The apparatus of claim 9, wherein said seventh logic is reconfigurable in real time to enable the location to which the comparison result is routed to be altered in real time.

16. The apparatus of claim 9, further comprising:

eighth logic, the eighth logic being configured to resolve said comparison result produced by said sixth logic into a single digital value and to output the single digital value from the eighth logic to the seventh logic for routing by the seventh logic.

17. The apparatus of claim 16, further comprising ninth logic, the ninth logic being configured to compare the single digital value received by the fourth logic with the single digital value received by the eighth logic to produce a complex comparison result.

18. The apparatus of claim 16, wherein the first, second, third, fourth, fifth, sixth and seventh logic are comprised in an application specific integrated circuit (ASIC).

19. The apparatus of claim 18, wherein the ASIC receives programming signals from a programmable processor, and wherein the first, second, third, fifth, sixth and seventh logic are re-configurable via the programming signals received by the ASIC.

20. The apparatus of claim 18, wherein the apparatus is utilized for interrogating bits data frames that have been formatted in accordance with a particular communications protocol and transmitted to said apparatus.

21. The apparatus of claim 1, wherein the apparatus is utilized for interrogating bits data frames that have been formatted in accordance with a particular communications protocol and transmitted to said apparatus.

22. The apparatus of claim 21, wherein the apparatus is incorporated into a network interface device.

23. A method for interrogating a data frame, the data frame comprising a plurality of bits, the method comprising the step of:

selecting a particular bit pattern in the data frame for interrogation;

comparing a selected bit comparison value to said bit pattern to produce a comparison result; and

determining a location to which the comparison result is to be routed, wherein one of the steps of selecting, comparing and determining is performed by logic that is reconfigurable to thereby enable one of said bit pattern, said bit comparison value and said location to be programmably altered.

24. The method of claim 22, wherein the particular bit pattern selected from the data frame for interrogation can be programmably altered in real time.

25. The method of claim 22, wherein the bit comparison value can be programmably altered in real time.

26. The method of claim 22, wherein the location to which the comparison result is routed can be programmably altered in real time.

27. The method of claim 26, further comprising the step of:

prior to determining step, resolving said comparison result into a single digital value such that the comparison result that is routed is the single digital value.

28. The method of claim 27, wherein the method is performed by an application specific integrated circuit (ASIC) that receives programming signals from a programmable processor, and wherein the programming signals programmably alter the particular bit pattern selected from the data frame for interrogation, the selected bit comparison value compared to said bit pattern, and the location to which the comparison result is routed.

29. The method of claim 28, wherein the ASIC is incorporated into a network interface card and is utilized for interrogating bits of data frames that have been formatted in accordance with a particular communications protocol.